1. A semiconductor structure comprising:

a gate electrode comprising a hafnium nitride layer overlying a dielectric layer on a substrate wherein a ratio of hafnium to nitride in said hafnium nitride layer is less than or equal to one; and

source and drain regions within said substrate adjacent to said gate electrode.

2. The structure according to Claim 1 wherein said dielectric layer comprises silicon dioxide.

3. The structure according to Claim 1 wherein said dielectric layer comprises a high dielectric constant gate dielectric material consisting of: zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates or crystalline oxide

4. The structure according to Claim 1 further comprising a capping layer on said gate electrode wherein said capping layer comprises metal.

5. The structure according to Claim 4 wherein said capping layer comprises tungsten or TaN .

6. The structure according to Claim 1 wherein said hafnium nitride layer forms a capping layer on an underlying metal layer and wherein said metal layer overlies said dielectric layer.

7. The structure according to Claim 6 wherein said metal layer comprises tungsten or tantalum nitride.

8. A method for fabricating a semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a hafnium nitride layer overlying said dielectric layer;

depositing a capping layer overlying said hafnium nitride layer;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form a gate

electrode; and

forming source and drain regions within said substrate adjacent to said gate electrode.

9. The method according to Claim 8 wherein said depositing of said hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target.

10 .The method according to claim 9 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

11.The method according to Claim 8 wherein said dielectric layer comprises HfO2 and is deposited at 400°C using a MOCVD cluster tool.

12. The method according to Claim 8 wherein said dielectric layer comprises HfO2 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in N2 ambient.

13. The method according to Claim 8 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

14 The method according to Claim 8 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrode.

15. The method according to Claim 8 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

16. A method for fabricating a semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a first metal layer overlying said dielectric layer;

patterning said first metal layer and said dielectric layer to form a gate electrode; and

forming source and drain regions within said substrate adjacent to said gate electrode.

17. The method according to Claim 16 wherein said depositing of said first metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form a hafnium nitride first metal layer.

18 .The method according to claim 17 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

19.The method according to Claim 16 wherein said dielectric layer comprises HfO2 and is deposited at 400°C using a MOCVD cluster tool.

20. The method according to Claim 16 wherein said dielectric layer comprises HfO2 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in N2 ambient.

21. The method according to Claim 17 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

22. The method according to Claim 17 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrode.

23. The method according to Claim 17 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

24. The method according to Claim 17 further comprising:

depositing a second metal capping layer overlying said first metal layer prior to said patterning wherein said second metal is different from said first metal.

25. The method according to Claim 24 wherein said first metal layer comprises tungsten or tantalum nitride and wherein said second metal layer comprises hafnium nitride.

26. The method according to Claim 24 wherein said first metal layer comprises hafnium nitride and wherein said second metal layer comprises tungsten or tantalum nitride.

27. The method according to Claim 24 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition.

28. A semiconductor structure comprising:

a gate dielectric layer on a substrate wherein said gate dielectric layer does not comprise silicon oxide;

a gate electrode comprising a hafnium nitride layer overlying said gate dielectric layer; and

source and drain regions within said substrate adjacent to said gate electrode.

29. The structure according to Claim 28 wherein said gate dielectric layer comprises zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates or crystalline oxide;

30. The structure according to Claim 29 further comprising a capping layer on said gate electrode wherein said capping layer comprises metal.

31. The structure according to Claim 30 wherein said capping layer comprises tungsten or TaN .

32. The structure according to Claim 28 wherein said hafnium nitride layer forms a capping layer on an underlying metal layer and wherein said metal layer overlies said gate dielectric layer.

33. The structure according to Claim 32 wherein said metal layer comprises tungsten or tantalum nitride.

34. The structure according to Claim 28 wherein a ratio of hafnium to nitride in said hafnium nitride layer is less than or equal to one.